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L4	L2 and l1	0	L4
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L1	(smallest adj1 cut) or min-cut	172	L1

END OF SEARCH HISTORY

L15: Entry 9 of 14 File: USPT Jan 14, 1997

DOCUMENT-IDENTIFIER: US 5594891 A
TITLE: Bus checking device and bus checking method

Brief Summary Text (16):
The present invention is directed to a bus checking device for checking a bus including of a tri-state element on the basis of information about a designed circuit for signal conflict or floating of the bus with control signals outputted from a bus control circuit for controlling the bus. According to the present invention, the bus checking device comprises checked control circuit extracting means for extracting a control circuit portion concerned in determination of the control signals from the information about the designed circuit according to a predetermined rule and exclusiveness checking means for checking exclusiveness of the bus by checking exclusiveness of output signals of the control circuit portion extracted by the checked control circuit extracting means.

Brief Summary Text (45):
The present invention is also directed to a bus checking method for checking a bus including a tri-state element on the basis of information about a designed circuit for signal conflict or floating of the bus with control signals outputted from a bus control circuit for controlling the bus. According to the present invention, the bus checking method comprises a checked control circuit extracting step for extracting a control circuit portion concerned with determination of the control signals from the information about the designed circuit according to a predetermined rule and an exclusiveness checking step for checking exclusiveness of the bus by checking output signals of the control circuit portion extracted in the checked control circuit extracting step.

CLAIMS:

1. A bus checking device for checking a bus including tri-state elements on the basis of information about a designed circuit for signal conflict or floating of said bus with control signals outputted from a bus control circuit for controlling said bus, comprising:

checked control circuit extracting means for extracting a control circuit portion which is concerned in determination of said control signals from said information about said designed circuit according to a predetermined rule; and

exclusiveness checking means for checking exclusiveness of said bus by checking exclusiveness of output signals of said control circuit portion extracted by said checked control circuit extracting means.

11. A bus checking method for checking a bus including tri-state elements on the basis of information about a designed circuit for signal conflict or floating of said bus with control signals outputted from a bus control circuit for controlling said bus, comprising:

a checked control circuit extracting step for extracting a control circuit portion which is concerned in determination of said control signals from said information about said designed circuit according to a predetermined rule; and

an exclusiveness checking step for checking exclusiveness of said bus by checking output signals of said control circuit portion extracted in said checked control circuit extracting step.

L15: Entry 12 of 14 File: USPT May 30, 1995

DOCUMENT-IDENTIFIER: US 5420871 A
TITLE: Method for maintaining bus integrity during testing

Detailed Description Text (12):
If the input I.sub.i is not found to be the output of an active high tri-state gate during step 30, then step 32 is executed and a determination is made whether the input I.sub.i is the output of an active low tri-state gate. In other words, a determination is made during step 32 whether the input I.sub.i is the output of a tri-state gate that is active when a logic low of "0" is applied on its control line c to enable the tri-state gate to pass the signal on its input line i to its output line o. Should the input I.sub.i not be the output of an active low tri-state gate, then execution of the bus-learning routine branches to step 34 whereupon BUS is designated as a potential conflict bus. As may be appreciated, if the input I.sub.i is not the output of either an active low or active high tri-state bus, than the input must be the output of some other device that cannot be controlled like a tri-state gate. Consequently, if the device supplying the input I.sub.i cannot be controlled like a tri-state gate, then a bus conflict is possible. Following step 34, step 36 is executed, and the bus-learning routine ends with respect to examination of the selected bus. (The bus-learning routine of FIG. 2 is now ready to be executed for the next selected bus.)

Other Reference Publication (1):
Y. Koseko, T. Ogihara, and S. Murai, "Tri-State Bus Conflict Checking Method for ATPG Using BDD", International Conference on Computer-Aided Design, Santa Clara, Calif., Nov., 1993.

CLAIMS:

2. The method according to claim 1 wherein a potential conflict on the bus is determined by the steps of:

initializing the circuit to unknown values;

successively determining whether each input to the bus comprises the output of a tri-state gate, and if not, then indicating that the bus is a potential conflict bus; and

implying, if possible, for each successive input to the bus which is established to be the output of a tri-state gate, logic values needed in the circuit which would cause the tri-state gate to be active;

determining whether implication of all logic values in the circuit is possible, and if not, then indicating that the bus is potential conflict bus; and

determining whether each bus input, other than the bus input established to be output of a tri-state gate, is a high-impedance value when the tri-state gate is active, and if not, designating the bus as a potential conflict bus,

otherwise, if all inputs to the bus, other that the input from the tri-state gate, are high impedance when the gate is active, then designating the bus as a no-

conflict bus.

L9: Entry 24 of 34 File: USPT Jan 14, 1997

DOCUMENT-IDENTIFIER: US 5594891 A
TITLE: Bus checking device and bus checking method

Brief Summary Text (3):
The present invention relates to a bus checking device and a bus checking method for checking for occurrence of signal conflict or floating on buses with tri-state element structure existing in logic circuits.

Brief Summary Text (5):
If buses with tri-state element structure existing in a logic circuit cause signal conflict or floating, large current may flow to cause destruction or deterioration of the device.

Brief Summary Text (16):
The present invention is directed to a bus checking device for checking a bus including of a tri-state element on the basis of information about a designed circuit for signal conflict or floating of the bus with control signals outputted from a bus control circuit for controlling the bus. According to the present invention, the bus checking device comprises checked control circuit extracting means for extracting a control circuit portion concerned in determination of the control signals from the information about the designed circuit according to a predetermined rule and exclusiveness checking means for checking exclusiveness of the bus by checking exclusiveness of output signals of the control circuit portion extracted by the checked control circuit extracting means.

Brief Summary Text (18):
In the bus checking device, since a control circuit portion concerned in determining control signals is extracted and the exclusiveness of output signals of the control circuit portion extracted by the checked control circuit extracting means is checked to check the exclusiveness of a bus, it has the effect that efficient and accurate checks can be made as to whether signal conflict and floating occur on the bus composed of tri-state elements.

Brief Summary Text (45):
The present invention is also directed to a bus checking method for checking a bus including a tri-state element on the basis of information about a designed circuit for signal conflict or floating of the bus with control signals outputted from a bus control circuit for controlling the bus. According to the present invention, the bus checking method comprises a checked control circuit extracting step for extracting a control circuit portion concerned with determination of the control signals from the information about the designed circuit according to a predetermined rule and an exclusiveness checking step for checking exclusiveness of the bus by checking output signals of the control circuit portion extracted in the checked control circuit extracting step.

Brief Summary Text (47):
In the bus checking method, since a control circuit portion concerned in determining control signals is extracted and output signals of that control circuit portion are checked to check the exclusiveness of the bus, it has the effect that efficient and accurate checks can be made as to whether signal conflict and

floating occur or not on buses composed of tri-state elements.

Detailed Description Text (101):
Next, the procedure of the case of realizing the above-described bus checking device using a computer will be described referring to FIGS. 32 through 34. It starts and first the signal conflict and floating of buses with the tri-state element structure is checked in the step S140. This process is a process of the exclusiveness check of buses done according to the procedure of the above-described first, second, third, fourth or fifth preferred embodiment.

CLAIMS:

1. A bus checking device for checking a bus including tri-state elements on the basis of information about a designed circuit for signal conflict or floating of said bus with control signals outputted from a bus control circuit for controlling said bus, comprising:

checked control circuit extracting means for extracting a control circuit portion which is concerned in determination of said control signals from said information about said designed circuit according to a predetermined rule; and

exclusiveness checking means for checking exclusiveness of said bus by checking exclusiveness of output signals of said control circuit portion extracted by said checked control circuit extracting means.

11. A bus checking method for checking a bus including tri-state elements on the basis of information about a designed circuit for signal conflict or floating of said bus with control signals outputted from a bus control circuit for controlling said bus, comprising:

a checked control circuit extracting step for extracting a control circuit portion which is concerned in determination of said control signals from said information about said designed circuit according to a predetermined rule; and

an exclusiveness checking step for checking exclusiveness of said bus by checking output signals of said control circuit portion extracted in said checked control circuit extracting step.

L9: Entry 31 of 34 File: USPT May 30, 1995

DOCUMENT-IDENTIFIER: US 5420871 A
TITLE: Method for maintaining bus integrity during testing

Detailed Description Text (12):
If the input I.sub.i is not found to be the output of an active high tri-state gate during step 30, then step 32 is executed and a determination is made whether the input I.sub.i is the output of an active low tri-state gate. In other words, a determination is made during step 32 whether the input I.sub.i is the output of a tri-state gate that is active when a logic low of "0" is applied on its control line c to enable the tri-state gate to pass the signal on its input line i to its output line o. Should the input I.sub.i not be the output of an active low tri-state gate, then execution of the bus-learning routine branches to step 34 whereupon BUS is designated as a potential conflict bus. As may be appreciated, if the input I.sub.i is not the output of either an active low or active high tri-state bus, than the input must be the output of some other device that cannot be controlled like a tri-state gate. Consequently, if the device supplying the input I.sub.i cannot be controlled like a tri-state gate, then a bus conflict is possible. Following step 34, step 36 is executed, and the bus-learning routine ends with respect to examination of the selected bus. (The bus-learning routine of FIG. 2 is now ready to be executed for the next selected bus.)

Other Reference Publication (1):
Y. Koseko, T. Ogihara, and S. Murai, "Tri-State Bus Conflict Checking Method for ATPG Using BDD", International Conference on Computer-Aided Design, Santa Clara, Calif., Nov., 1993.

CLAIMS:

2. The method according to claim 1 wherein a potential conflict on the bus is determined by the steps of:

initializing the circuit to unknown values;

successively determining whether each input to the bus comprises the output of a tri-state gate, and if not, then indicating that the bus is a potential conflict bus; and

implying, if possible, for each successive input to the bus which is established to be the output of a tri-state gate, logic values needed in the circuit which would cause the tri-state gate to be active;

determining whether implication of all logic values in the circuit is possible, and if not, then indicating that the bus is potential conflict bus; and

determining whether each bus input, other than the bus input established to be output of a tri-state gate, is a high-impedance value when the tri-state gate is active, and if not, designating the bus as a potential conflict bus,

otherwise, if all inputs to the bus, other that the input from the tri-state gate, are high impedance when the gate is active, then designating the bus as a no-

conflict bus.